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GaAs MESFET Optimization and New Device Applications based on Wave Property Studies

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Abstract

The results to be presented are obtained by an experimental investigation of the wave properties on FET structures using especially fabricated MeSFETs. The use of this information for an optimization of MeSFET structures and for a development of new devices is discussed. It will be demonstrated that a significant improvement of the FET gain is obtainable.

Introduction

The gate width of an FET is limited by the gate attenuation constant, the different phase constants of gate and drain electrodes and reflections at the open ends of these electrodes. Due to these effects the gain of the FET reaches an optimum value at a certain gate length | 1 |. To overcome such problems a usual approach is to parallel many short gates. The disadvantage of this is low input and output impedances which decrease with the number of parallel FETs. Therefore an especially constructed FET with a gate width of 3200 µm and a gate length of 10 µm was constructed which has connecting pads on each end of the gate and drain electrodes (Fig. 1). This makes it possible to measure the 4-port S-parameters of the device.

Using this data our aim is to compute the optimum terminations for the normally open ends of gate and drain electrodes to improve the gain of the transistor. In fact, this optimization can be combined with the approach in which many FETs are connected in parallel. Further, the attenuation and phase constants and the characteristic impedances for gate and drain electrode were computed. The measurement of these constants offers the possibility to propose new devices like
- voltage controlled phase shifters for high frequencies and
- tunable attenuators.

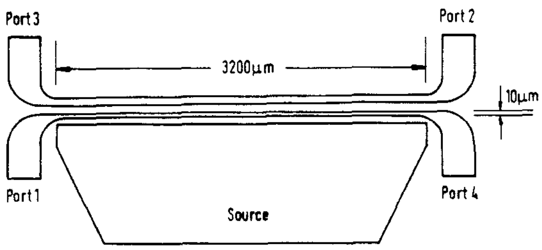

Fig. 1 Schematic top view of the FET

The MESFET Test Structures

The FET was fabricated on epitaxial material with a doping density of $1 \times 10^{17}/cm^3$, and a thickness of 0.4 µm was used. The active area is defined by a mesa structure. Ohmic contacts were evaporated consisting of a Au : Ge/Ni layer with thickness of 700 Å for Au : Ge and 300 Å. for Ni. Subsequently the contacts were sintered at 460°C in a N_2 atmosphere. The active channel was etched in an $NaOH$-H_2O_2 solution. Aluminium with a thickness of 2000 Å acts as gate material.

The Propagation Constants and Characteristic Impedances

4-port S-parameters were measured in the frequency range from 0.1 to 2 GHz using a HP-network analyser. The characteristic impedances and the propagation constant of the waves on the gate and drain in the direction along the electrode width were computed from these results. Fig. 2 gives the slowing factor β/β_0 of gate and drain lines versus frequency in dependance of the gate-source voltage U_{GS}. For comparison, theoretical curves are also presented, based on a program developed by Heinrich |3.4| by using an orthogonal function approach, for a FET with the same dimension and U_{GS} = 2 V. The agreement is particularly good for the gate line. The slowing factor of the gate line is higher and depends much more on U_{GS} than that of the drain line. This effect can be used to fabricate very fast voltage tuned phase shifters especially for the higher frequencies |5|, by connecting the input and output to the two opposite ends of the drain (or gate), with the modulation signal applied to the other electrode. Fig. 3 shows the attenuation constants α where the behaviour of the gate line is described particularly satisfactorily by the thery. The α of the drain line is increasing when the depletion layer under the gate becomes thin, because in this case the shunt resistance of the drain line is low. A voltage dependent attenuator as proposed by Hughes | 5| can be considered to be a realistic possibility by connecting the input, output and modulation signal in a similar manner as the above phase shifter, but by operating at different bias ranges.

Fig. 4 presents the characteristic impedances as derived from the 4-port S-parameters.

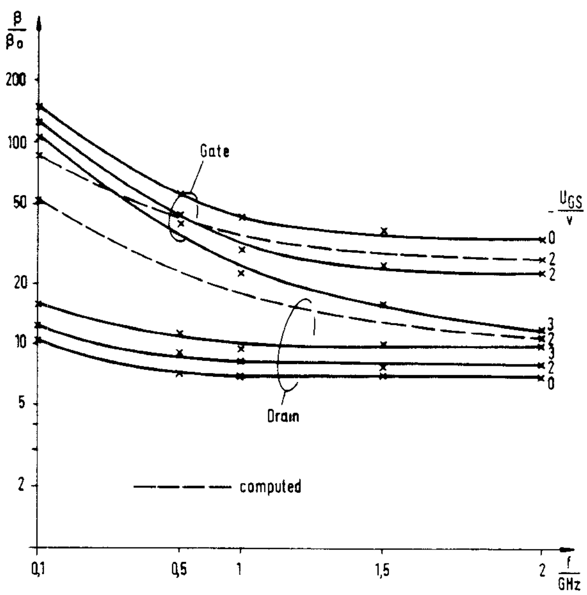

Fig. 2 Slowing factor versus frequency

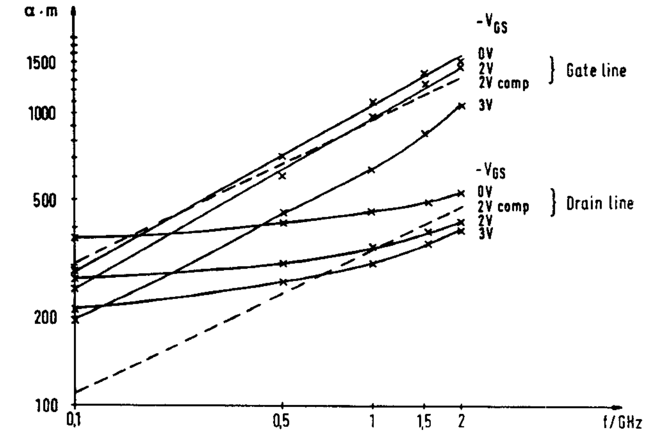

Fig. 3 Attenuation constant α versus frequency and gate source voltage U_{GS}

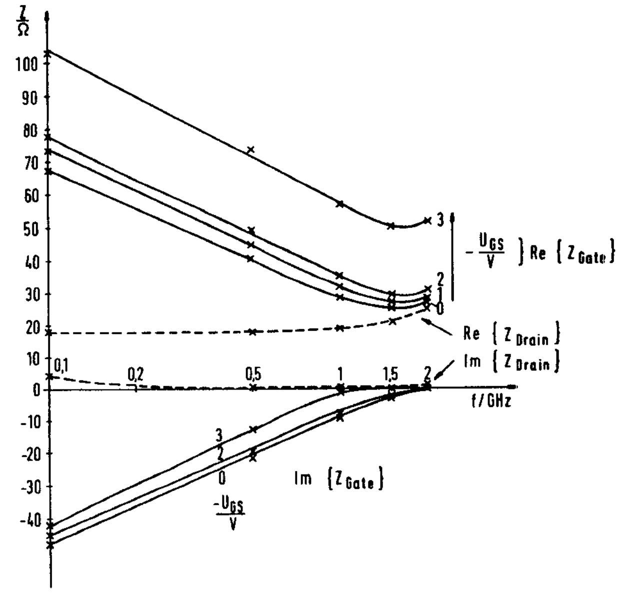

Fig. 4 Characteristic impedance versus frequency and gate source voltages U_{GS}

Optimization by suitably Terminating the normally free electrode ends

A method is proposed which gives the optimum terminations of the normally free electrode ends. The 4-port S-parameters are used to compute the resulting S-parameters of the remaining 2-port (port 1 - port 2) if the normally open ends are connected to terminations. These calculations were then experimentally verified by producing the terminations by tunable loads. The results are in very good agreement with the theoretical values. These 2-port S-parameters make it possible to compute the MAG (maximum available gain) and Rollet's constant K. The best MAG was obtained for complex terminations at the previously free ends of gate line (port 3) and drain line (port 4). In Fig. 5 and 6 the MAG is presented as a function of the angles of the reflection coefficients r_3 and r_4 at ports 3 and 4, respectively. From Fig.5 it is obvious that not the normally employed open circuit but an inductor ($\sphericalangle r_3 \approx 36^0$) employed at port 3 gives the best MAG. The MAG is improved in this case from 6.2 dB to 10.6 dB.

Fig. 6 shows that the termination at the end of the drain line, i.e. port 4, can be chosen in a wide range without degrading the MAG. Results are to be presented concerning possibilities of thin-film realizations of suitable electrode-end loading.

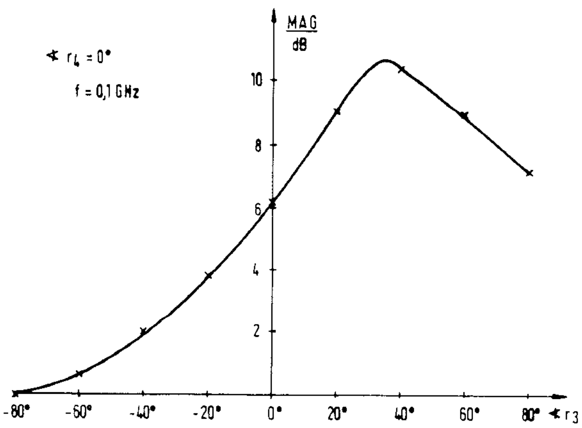

Fig. 5 MAG versus the angle of the reflection coefficent at port 3 ($\sphericalangle r_4 = 0^0$)

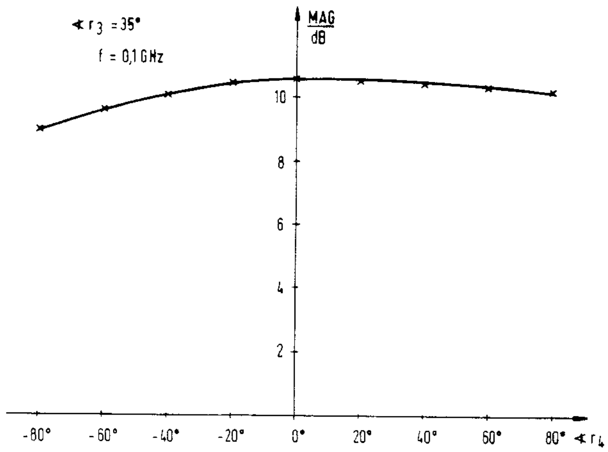

Fig. 6 MAG versus the angle of the reflection coefficient at port 4 ($\sphericalangle r_3 = 35^0$)

Conclusion

The effect of a voltage dependent phase and attenuation constant on the gate line can be used to fabricate

- fast voltage dependent phase-shifters and phase modulators
- tunable attenuators.

Employing optimum terminations at the normally open ends of gate and drain lines leads to a significant improvement of the gain of a FET amplifier.

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